UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/688,826 | 10/17/2003 | Juergen Luebbe | TI-35437 | 2376 |

7590 12/29/2004

Dan Swayze
Texas Instruments Incorporated
M/S 3999
P. O. Box 655474
Dallas, TX 75265

| EXAMINER | |
|---|---|
| MCCLOUD, RENATA D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2837 | |

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/688,826 | LUEBBE, JUERGEN | |
| | Examiner | Art Unit | |
| | Renata McCloud | 2837 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "sensing unit", "cancellation circuit", and the "generation unit" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show C21, C22, phase 1, phase 2, as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

3. The drawings are objected to because referring to Fig. 1, it is unclear what 11 and 13 are pointing to. In Fig. 2, it is unclear what 25, 26, 22 are pointing to. In Fig. 3, it is unclear what 31, 25, 26, 22, 32 are pointing to. In Fig. 4, it is unclear what 25,26,31,32,22 are pointing to. The arrows should be touching the object it is pointing to. Also, some of the characters in the drawings are too small and unclear to be read, such as the wording around the capacitors and the switches. For example, in Fig. 1, it is unclear what the objects within the VCM are and it is unclear what the wording is around the VCM. In Fig. 2, the small wordings around the capacitors are illegible. Some of the reference numbers are illegible. For example, in Fig. 4, 42A and 42B are unclear.

4. The drawings are objected to because the interconnections between the figures are not shown. For example, Figures 2-3 are SC controllers, however it is unclear how they are connected in relation to Figure 1.

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The limitations "sensing unit", "generation unit" and "cancellation circuit" are not in the specification.

### *Claim Objections*

6. Claims 11 objected to because of the following informalities: the limitation "said proportion part" should be "said proportional part". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 2, 3, 6-9, 12-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 2 and 12: how the analog type response has a resolution free of ripple about the target voltage is not enabled.

Claims 3 and 13: how the compensation signal is characterized by a voltage step proportional with an infinite resolution approaching the target voltage over a constant time period is not enabled.

Claims 6 and 14: the specification does not disclose what the "cancellation circuit", or the "sensor unit" is, so it is not enabled how they are connected. It is also unclear how such a connection cancels the DC offset.

Claims 7 and 15: the specification does not disclose what the "cancellation circuit", or the "sensor unit" is, so it is not enabled how they are connected. It is also unclear how such a connection cancels the DC offset.

Claims 8 and 16: the specification does not disclose what the "cancellation circuit", or the "sensor unit" is, so it is not enabled how they are connected. It is also not enabled how such a connection determines the DC offset or cancels the DC offset.

Claim 9: it is not disclosed in the specification that the DC offset is determined prior to sensing the voltage.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Brito et al (US 6040671).

**Claims 1:** an apparatus comprising a sensing unit (Fig. 4: 116) sensing a voltage corresponding to a voltage across the coil and providing a first signal indicative of the velocity; a generation circuit (Fig. 4: 92) providing a second signal indicative of a target voltage corresponding to a target velocity; and a controller (Fig. 4: 100/102/104) receiving the first signal and the second signal and determining a compensation signal characterized as an analog response to the target voltage and for effectuating the velocity (Col. 4:21-45).

**Claim 2:** as best understood, the compensation signal is an analog response regulated to the target voltage with a resolution free of ripple about the target voltage (Fig. 6).

**Claim 3:** as best understood, the compensation signal is characterized by a voltage step proportional to an error with an infinite resolution approaching the target voltage over a time period (Col. 4:58-4:10, the compensation signal is a result of the error voltage).

**Claim 4:** the controller includes a first node (Fig. 4: 98) for receiving the first signal (Fig. 4: signal from 116) and the second signal (signal from 92) and determining a difference (98 takes the difference) therebetween and providing the difference to a proportional part (Fig. 4:100) and an integrator part (102); the integrator part (102) providing a third signal indicative of a mathematical integration of the difference and the

proportional part (148) providing a fourth signal indicative of a multiple of the difference; and the controller (Fig. 4: 100/102/104) having a summing node (104) receiving the third signal and the fourth signal and responsive for determining a summed signal which corresponds to the compensation signal (104 produces 106).

**Claim 5:** the third signal (signal from 102) is a voltage signal characterized by a voltage step proportional to an error (the input to 102 is the error from 98).

**Claim 6:** as best understood, a cancellation circuit (Fig. 6) coupled with the sensing unit (116) and the integrator part (102) for canceling dc offset (Col. 8:11-50).

**Claim 7:** as best understood, a cancellation circuit (Fig. 6) coupled to the sensing unit (116) and operable for determining a dc offset and providing the dc offset to the integrator part (102) for the mathematical integration for canceling the dc offset from the compensation signal (Col. 8:11-50).

**Claim 8:** as best understood, a cancellation circuit (Fig. 6) coupled to the sensing unit (116) and the integrator (102) and operable for determining a dc offset of the sensing unit and the integrator and providing the dc offset to the integrator part for the mathematical integration for canceling the dc offset from the compensation signal.

**Claim 9:** as best understood, the dc offset is determined prior to sensing the coil voltage (the offset is determined in Fig. 6).

**Claim 10:** an amplifier unit (Fig. 4:108) having an input for receiving the compensation signal and responsive for providing a corresponding current for application to the coil.

**Claim 11:** an apparatus comprising a first input (Fig. 4: input to 116) receiving a first signal corresponding to the voltage sensed across the coil (Fig. 4: 68); a second input (Fig. 4: input at 92) receiving a second signal indicative of a target voltage (Fig. 4: VR); a node receiving the first signal and second signal (Fig. 4: 98) and determining a difference and providing the difference to a proportional part (Fig. 4: 100) and an integrator part (Fig. 4: 102); the integrator proving a third signal (100) and the proportional part providing a fourth signal (102); a summing node (Fig. 4: 104) receiving the third and fourth signals and determining a compensation signal from the sum of the third and fourth signals (Fig. 4: 106; Col. 4:45-5:10; Col. 5:34-56).

**Claim 12:** as best understood, the compensation signal is an analog response regulated to the target voltage with a resolution free of ripple about the target voltage (Fig. 6: 176).

**Claim 13:** as best understood, the compensation signal (Fig. 4: signal from 104) is characterized by a voltage step proportional to an error with an infinite resolution approaching the target voltage over a time period (the signal from 104 is a result of the error voltage from 98).

**Claim 14:** as best understood, a cancellation circuit (Fig. 6) coupled to the sensing circuit and the integrator for canceling the dc offset.

**Claim 15:** as best understood, a cancellation circuit (Fig. 6) coupled to the sensing unit (116) and operable for determining a dc offset and providing the dc offset to the integrator part (102) for the mathematical integration for canceling the dc offset from the compensation signal (Fig. 6).

**Claim 16:** as best understood, a cancellation circuit (Fig. 6) coupled to the sensing unit (116) and the integrator (102) and operable for determining a dc offset of the sensing unit and the integrator and providing the dc offset to the integrator part for the mathematical integration for canceling the dc offset from the compensation signal (Fig. 6).

11. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakatani et al (US 6388416).

**Claim 1:** an apparatus comprising a sensing unit (Fig. 33: 18) sensing a voltage corresponding to a voltage across the coil and providing a first signal indicative of the velocity; a generation circuit (Fig. 33: 19) providing a second signal indicative of a target voltage corresponding to a target velocity; and a controller (Fig. 33: 11) receiving the first signal and the second signal and determining a compensation signal characterized as an analog response to the target voltage and for effectuating the velocity.

**Claim 2:** as best understood, the compensation signal is an analog response regulated to the target voltage with a resolution free of ripple about the target voltage (Fig. 39).

**Claim 3:** as best understood, the compensation signal is characterized by a voltage step proportional to an error with an infinite resolution approaching the target voltage over a time period (Fig. 39).

**Claim 4:** the controller includes a first node (Fig. 33: 10) for receiving the first signal (Fig. 33: signal from 18) and the second signal (signal from 19) and determining a difference therebetween and providing the difference to a proportional part (Fig. 33:11; Fig. 13A: 110) and an integrator part (Fig. 13A: 112); the integrator part (Fig. 13A: 112) providing a third signal indicative of a mathematical integration of the difference and the proportional part (Fig. 13A: 110) providing a fourth signal indicative of a multiple of the difference; and the controller (Fig. 33: 11) having a summing node (Fig. 13A: 114 ) receiving the third signal and the fourth signal and responsive for determining a summed signal which corresponds to the compensation signal (Fig. 13A: 114 sums 110 and 112).

**Claim 5:** the third signal (Fig. 13A: signal from 112) is a voltage signal characterized by a voltage step proportional to an error (the signal comes from the error data).

**Claim 6:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled with the sensing unit (Fig. 33: 18) and the integrator part (Fig. 13A: 112) for canceling dc offset (Col. 26:5-33).

**Claim 7:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled to the sensing unit (Fig. 33: 18) and operable for determining a dc offset and providing the dc offset to the integrator part (Fig. 13A: 112) for the mathematical integration for canceling the dc offset from the compensation signal.

**Claim 8:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled to the sensing unit (fig. 33:18) and the integrator (fig. 13A: 112) and operable for determining a

dc offset of the sensing unit and the integrator and providing the dc offset to the integrator part for the mathematical integration for canceling the dc offset from the compensation signal.

**Claim 9:** as best understood, the dc offset is determined prior to sensing the coil voltage (Fig. 13A: 111).

**Claim 10:** an amplifier unit (Fig. 19: 204) having an input for receiving the compensation signal and responsive for providing a corresponding current for application to the coil.

**Claim 11:** an apparatus comprising a first input (Fig. 33: from 18) receiving a first signal corresponding to the voltage sensed across the coil; a second input (Fig. 33: input at 19) receiving a second signal indicative of a target voltage; a node (Fig. 33: 10) receiving the first signal and second signal and determining a difference and providing the difference to a proportional part (Fig. 33:11; Fig. 13A: 110) and an integrator part (Fig. 33: 11; Fig. 13A: 112); the integrator (Fig. 13A: 112) providing a third signal and the proportional part (Fig. 13A: 110) providing a fourth signal; a summing node (Fig. 13A: 114) receiving the third and fourth signals and determining a compensation signal (Fig. 13A: signal from 114) from the sum of the third and fourth signals.

**Claim 12:** as best understood, the compensation signal is an analog response regulated to the target voltage with a resolution free of ripple about the target voltage (Fig. 39)

**Claim 13:** as best understood, the compensation signal is characterized by a voltage step proportional to an error with an infinite resolution approaching the target voltage over a time period (Fig. 39).

**Claim 14:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled to the sensing circuit and the integrator for canceling the dc offset.

**Claim 15:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled to the sensing unit and operable for determining a dc offset and providing the dc offset to the integrator part for the mathematical integration for canceling the dc offset from the compensation signal.

**Claim 16:** as best understood, a cancellation circuit (Fig. 13A: 111) coupled to the sensing unit (Fig. 33: 18) and the integrator (Fig. 13A: 112) and operable for determining a dc offset of the sensing unit and the integrator and providing the dc offset to the integrator part for the mathematical integration for canceling the dc offset from the compensation signal.

## *Conclusion*

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renata McCloud whose telephone number is (571) 272-2069. The examiner can normally be reached on Mon.- Fri. from 8 am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on (571) 272-2800 ext. 4. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Renata McCloud
Examiner
Art Unit 2837

RDM